Final Exam
Digital System Design

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Marks: 100 Time: 3 hrs

(This exam is designed for OPEN BOOK & OPEN NOTES)

Q1. **Marks 25 = 15 + 10 (Take home)**

Design a string matcher for a byte interface. The design takes an 8 character reference string (64-bit) as input. On the byte interface, the design gets a byte of data at every *posedge* of clock. The design generates a 1 at the output if string is matched with the input reference string. Draw RTL diagram of the design and write RTL Verilog code of its implementation. Also write stimulus to test the working of your design. (Copy your code on a separate sheet for take home exam. Take your time to code and simulate YOUR CODED design using any Verilog simulator and demonstrate your implementation with the Semester project.)

Q2. **Marks 10**

Design a state machine to implement a Medium Access Control (MAC) Protocol for a wireless communication network. Draw a bubble diagram to show your design. The protocol should implement the following:

(a) Any node to transmit first checks that no other node in its range is transmitting.
(b) If the node detects any transmission, it waits for the transmission to end.
(c) The node then sends a *req* to the destination node and then waits for the *ack* from the destination node.
(d) If the node does not receive any *ack*, then it waits for 10 ms and if there is no other transmission in its range, sends the *req* again and keeps repeating this sequence three times before dropping the current transmission to the destination with a message destination is not in range.
(e) In case the destination sends an *ack*, the node transmits a packet of data to the destination and then waits for the *ack_packet* from the destination node. After receiving *ack_pack* it silently receives any transmission meant for the node or let other nodes in the network to transmit.

(f) After transmitting one packet If the node needs to transmit any other packet, it waits for 60 ms and only then serves the request of transmission of a new packet of data in the network.

Q3. **Marks 25=(8,10,7)**

Design a micro coded state machine that optimally implements the following micro codes

$C_k = A_i \pm B_j$
$C_k = A_i \ \& \ B_j$
$C_k = A_i \times B_j$
$A_i = C_j$
$B_i = C_j$
Jump LABEL,
If (!Z) Jump LABEL
If (N) Jump LABEL
Call Subroutine at LABEL

Where A, B and C are three register files with four registers each where i,j,k ϵ {0,1,2,3}, and all the registers are 8-bit wide. If the result of an arithmetic and logic micro code is zero or negative it sets the zero-flag (Z) or negative-flag (N) respectively. Assume Program Memory (PM) is 256 deep. The LABEL is any legal address in the PM. Assume all operands are 8-bit Q1.7 format signed numbers. The multiplication micro code performs fractional (signed x signed) multiplication and only keeps 8 MSB of the product.

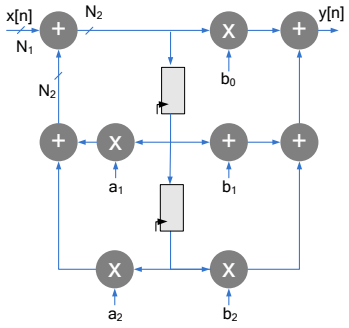
(a) Draw RTL diagram for the design of the datapath and the controller. Clearly identify all control signals and their widths.
(b) Write RTL Verilog code of the Datapath ONLY
(c) Give micro code format for your design by giving width of different fields in the micro-code.

Q4. **Marks 40=(5,5,5,5,5,7,8)**

(a) Add two 12 bit numbers A and B using Carry Skip Adder logic.
A = 1011_ 1010_1011
B = 1101_0101_1101
(b) Compute correction vector for sign extension elimination while computing A+B-C using a compression tree where A, B and C are three signed numbers in Q1.7, Q7.1 and Q3.2 format respectively.
(c) Compute Value of K for a four stage CORDIC algorithm.
(d) Compute control word W for generating 1 MHz frequency cosine and sine where clock frequency of the design is 100 MHz and the accumulator register is 18-bit wide.

(e) Convert -0.001797 floating point number into Q1.15 format and then change the fixed point number to CSD representation.

(f) Unfold the following design by a factor of 3.



(g) Design a **micro-program memory** based controller for traffic signal in a crossing where a minor road with seldom traffic crosses a main highway. The controller checks if there are no cars on the minor road, it keeps green light on the main road ON. In case it detects a car on the minor road, it switches the lights on the main road to red and minor road to green for 20 seconds and then turns the lights back again.